High Output Current Differential Driver

AD815

FEATURES

Flexible Configuration
- Differential Input & Output Driver or Two Single-Ended Drivers

High Output Power
- Power Package
  - 26 dBm Differential Line Drive for ADSL Application
  - 40 V p-p Differential Output Voltage, R_L = 50 Ω
  - 500 mA Minimum Output Drive/Amp, R_L = 5 Ω
- Thermally Enhanced SOIC
  - 200 mA Minimum Output Drive/Amp, R_L = 10 Ω

Low Distortion
- –66 dB @ 1 MHz THD, R_L = 200 Ω, V_{OUT} = 40 V p-p
- 0.05% & 0.45° Differential Gain & Phase, R_L = 25 Ω (6 Back-Terminated Video Loads)

High Speed
- 120 MHz Bandwidth (–3 dB)
- 900 V/μs Differential Slew Rate
- 70 ns Settling Time to 0.1%

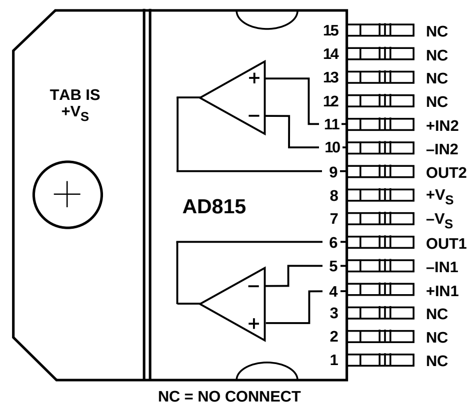
Thermal Shutdown

APPLICATIONS

- ADSL, HDSL & VDSL Line Interface Driver
- Coil or Transformer Driver
- CRT Convergence & Astigmatism Adjustment
- Video Distribution Amp
- Twisted Pair Cable Driver

FUNCTIONAL BLOCK DIAGRAM

15-Pin Through-Hole SIP (Y) & Surface-Mount DDPAK(VR)



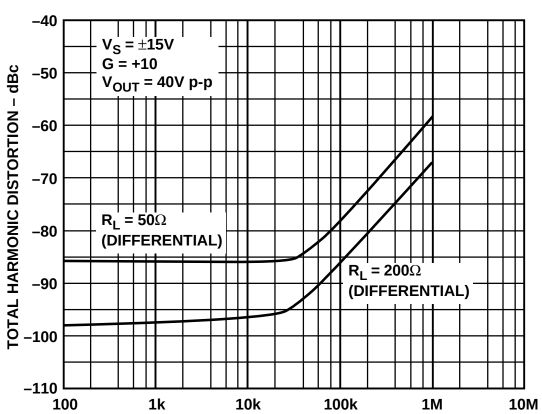
NC = NO CONNECT
REFER TO PAGE 3 FOR 24-PIN SOIC PACKAGE

PRODUCT DESCRIPTION

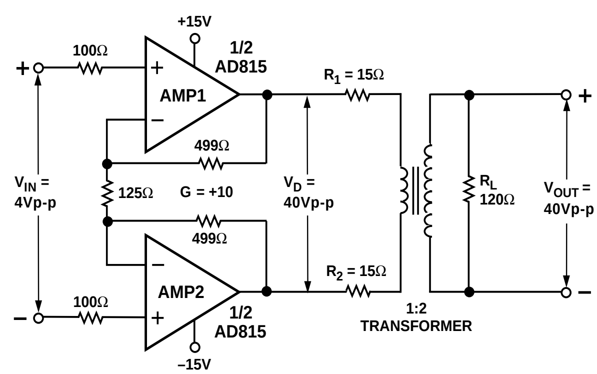
The AD815 consists of two high speed amplifiers capable of supplying a minimum of 500 mA. They are typically configured as a differential driver enabling an output signal of 40 V p-p on ±15 V supplies. This can be increased further with the use of a coupling transformer with a greater than 1:1 turns ratio. The low harmonic distortion of –66 dB @ 1 MHz into 200 Ω combined with the wide bandwidth and high current drive make the differential driver ideal for communication applications such as subscriber line interfaces for ADSL, HDSL and VDSL.

The AD815 differential slew rate of 900 V/μs and high load drive are suitable for fast dynamic control of coils or transformers, and the video performance of 0.05% & 0.45° differential gain & phase into a load of 25 Ω enable up to 12 back-terminated loads to be driven.

Three package styles are available, and all work over the industrial temperature range (–40°C to +85°C). Maximum driver performance is achieved with the power package available as through hole (Y) and surface-mount (VR), while the 24-pin SOIC (RB) driver performance is reduced due to the smaller package which has a higher thermal resistance.



Total Harmonic Distortion vs. Frequency



Subscriber Line Differential Driver

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD815–SPECIFICATIONS (@ T_A = +25°C, V_S = ±15 V dc, R_{FB} = 1 kΩ and R_{LOAD} = 100 Ω unless otherwise noted)

Model	Conditions	V_S	AD815A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Small Signal Bandwidth (–3 dB)	G = +1	±15	100	120		MHz
	G = +1	±5	90	110		MHz
Bandwidth (0.1 dB)	G = +2	±15		40		MHz
	G = +2	±5		10		MHz
Differential Slew Rate	V_{OUT} = 20 V p-p, G = +2	±15	800	900		V/µs
Settling Time to 0.1%	10 V Step, G = +2	±15		70		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f = 1 MHz, R_{LOAD} = 200 Ω, V_{OUT} = 40 V p-p	±15		–66		dBc
Input Voltage Noise	f = 10 kHz, G = +2 (Single Ended)	±5, ±15		1.85		nV/√Hz
Input Current Noise (+I_{IN})	f = 10 kHz, G = +2	±5, ±15		1.8		pA/√Hz
Input Current Noise (–I_{IN})	f = 10 kHz, G = +2	±5, ±15		19		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_{LOAD} = 25 Ω	±15		0.05		%
Differential Phase Error	NTSC, G = +2, R_{LOAD} = 25 Ω	±15		0.45		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5		5	8	mV
		±15		10	15	mV
	T_{MIN} – T_{MAX}				30	mV
Input Offset Voltage Drift				20		µV/°C
Differential Offset Voltage		±5		0.5	2	mV
		±15		0.5	4	mV
	T_{MIN} – T_{MAX}				5	mV
Differential Offset Voltage Drift				10		µV/°C
–Input Bias Current		±5, ±15		10	90	µA
	T_{MIN} – T_{MAX}				150	µA
+Input Bias Current		±5, ±15		2	5	µA
	T_{MIN} – T_{MAX}				5	µA
Differential Input Bias Current		±5, ±15		10	75	µA
	T_{MIN} – T_{MAX}				100	µA
Open-Loop Transresistance		±5, ±15	1.0	5.0		MΩ
	T_{MIN} – T_{MAX}		0.5			MΩ
INPUT CHARACTERISTICS						
Differential Input Resistance	+Input	±15		7		MΩ
	–Input			15		Ω
Differential Input Capacitance		±15		1.4		pF
Input Common-Mode Voltage Range		±15		13.5		±V
		±5		3.5		±V
Common-Mode Rejection Ratio	T_{MIN} – T_{MAX}	±5, ±15	57	65		dB
Differential Common-Mode Rejection Ratio	T_{MIN} – T_{MAX}	±5, ±15	80	100		dB
OUTPUT CHARACTERISTICS						
Voltage Swing	Single Ended, R_{LOAD} = 25 Ω	±15	11.0	11.7		±V
		±5	1.1	1.8		±V
	Differential, R_{LOAD} = 50 Ω	±15	21	23		±V
	T_{MIN} – T_{MAX}	±15	22.5	24.5		±V
Output Current[1, 2]						
VR, Y	R_{LOAD} = 5 Ω	±15	500	750		mA
		±5	350	400		mA
RB-24	R_{LOAD} = 10 Ω	±15	200	250		mA
Short Circuit Current		±15		1.0		A
Output Resistance		±15		13		Ω
MATCHING CHARACTERISTICS						
Crosstalk	f = 1 MHz	±15		–65		dB
POWER SUPPLY						
Operating Range[3]	T_{MIN} – T_{MAX}				±18	V
Quiescent Current		±5		23	30	mA
		±15		30	40	mA
	T_{MIN} – T_{MAX}	±5			40	mA
		±15			55	mA
Power Supply Rejection Ratio	T_{MIN} – T_{MAX}	±5, ±15	–55	–66		dB

NOTES

[1]Output current is limited in the 24-pin SOIC package to the maximum power dissipation. See absolute maximum ratings and derating curves.

[2]See Figure 12 for bandwidth, gain, output drive recommended operation range.

[3]Observe derating curves for maximum junction temperature.

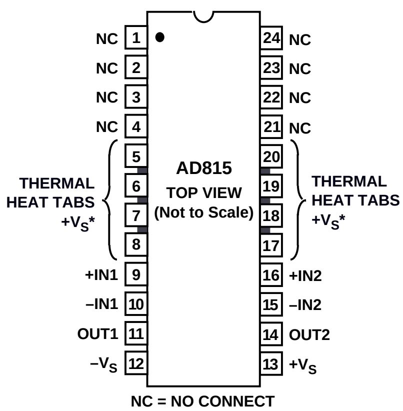
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V Total
Internal Power Dissipation[2]
Plastic (Y & VR) . . . 3.05 Watts (Observe Derating Curves)
Small Outline (RB) . . 2.4 Watts (Observe Derating Curves)
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±6 V
Output Short Circuit Duration
. . . . Observe Power Derating Curves
Can Only Short to Ground
Storage Temperature Range
Y, VR & RB Package . . . . –65°C to +125°C
Operating Temperature Range
AD815A . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air with 0 ft/min air flow: 15-Pin Through Hole and Surface Mount: θ_{JA} = 41°C/Watt; 24-Pin Surface Mount: θ_{JA} = 52°C/Watt.

PIN CONFIGURATION
24-Pin Thermally-Enhanced SOIC (RB-24)



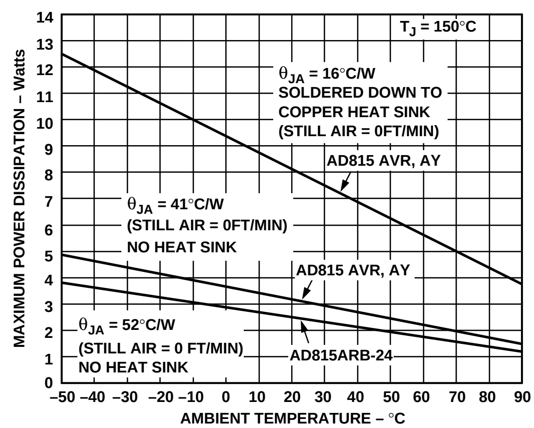
*HEAT TABS ARE CONNECTED TO THE POSITIVE SUPPLY.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD815 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

The AD815 has thermal shutdown protection, which guarantees that the maximum junction temperature of the die remains below a safe level, even when the output is shorted to ground. Shorting the output to either power supply will result in device failure. To ensure proper operation, it is important to observe the derating curves and refer to the section on power considerations.

It must also be noted that in high (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.



Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD815AY	–40°C to +85°C	15-Pin Through Hole SIP with Staggered Leads	Y-15
AD815AVR	–40°C to +85°C	15-Pin Surface Mount DDPAK	VR-15
AD815ARB-24	–40°C to +85°C	24-Pin Thermally Enhanced SOIC	RB-24
AD815ARB-24-REEL	–40°C to +85°C	24-Pin Thermally Enhanced SOIC	RB-24

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD815 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD815–Typical Performance Characteristics

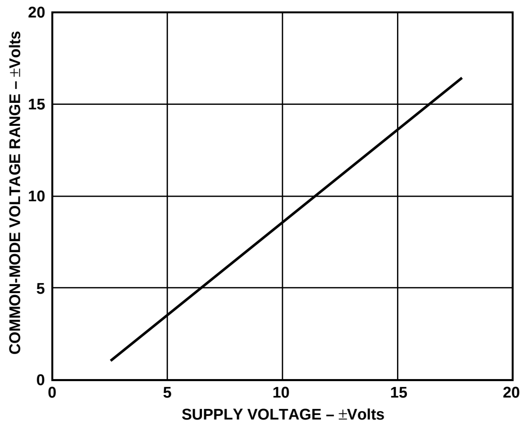


Figure 1. Input Common-Mode Voltage Range vs. Supply Voltage

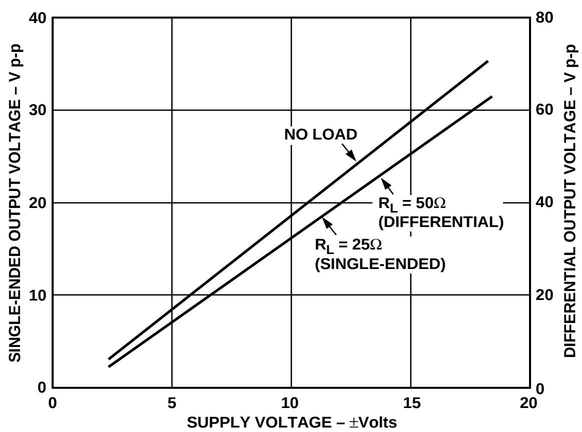


Figure 2. Output Voltage Swing vs. Supply Voltage

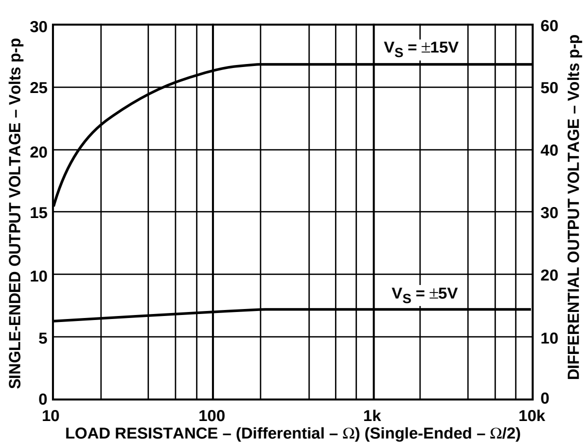


Figure 3. Output Voltage Swing vs. Load Resistance

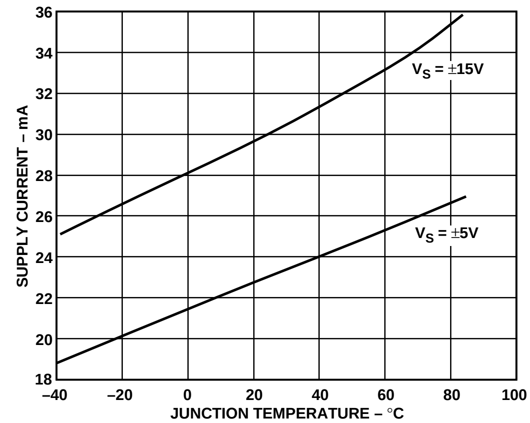


Figure 4. Total Supply Current vs. Temperature

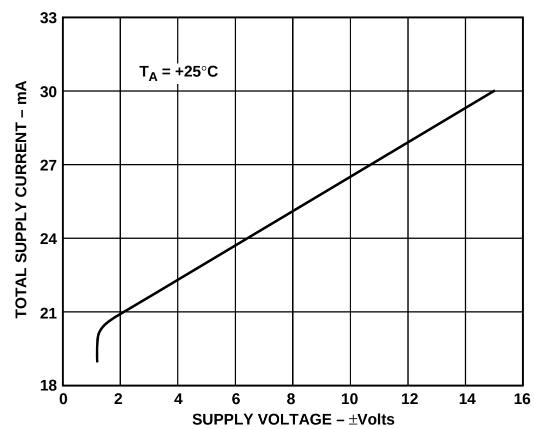


Figure 5. Total Supply Current vs. Supply Voltage

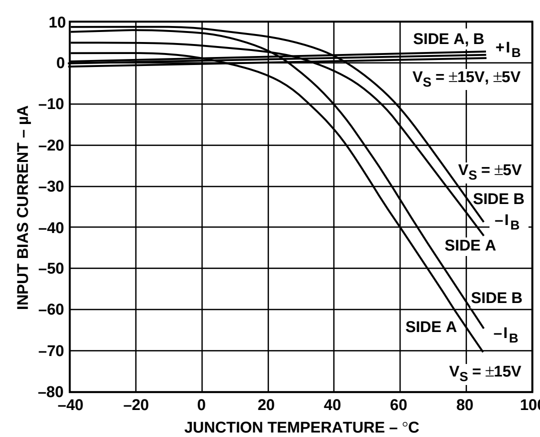


Figure 6. Input Bias Current vs. Temperature

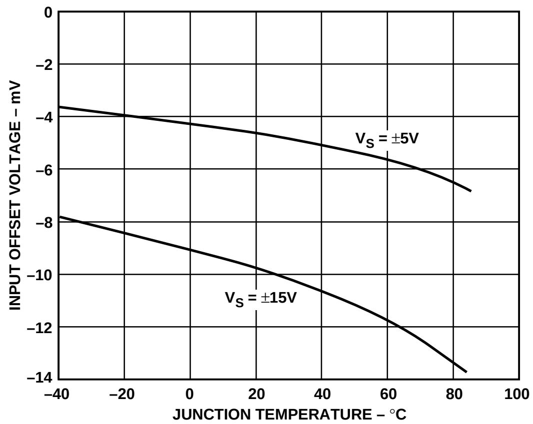


Figure 7. Input Offset Voltage vs. Temperature

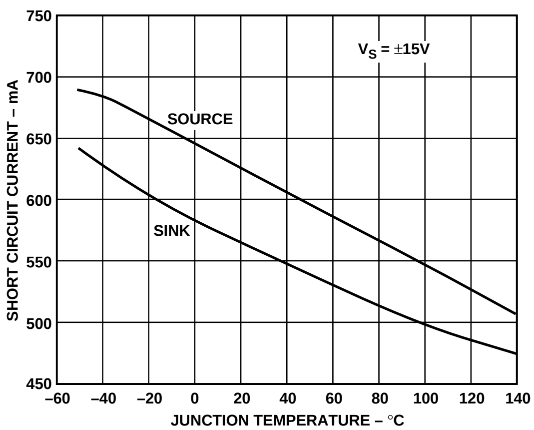


Figure 8. Short Circuit Current vs. Temperature

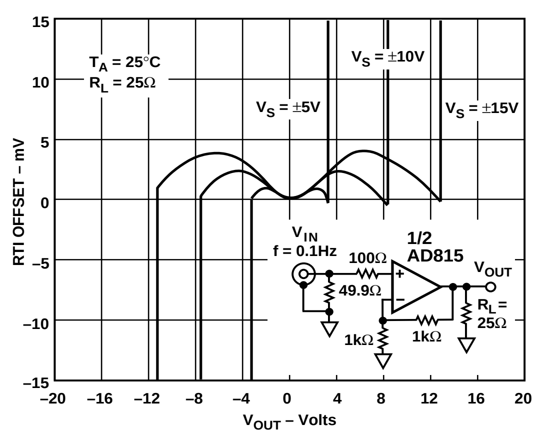


Figure 9. Gain Nonlinearity vs. Output Voltage

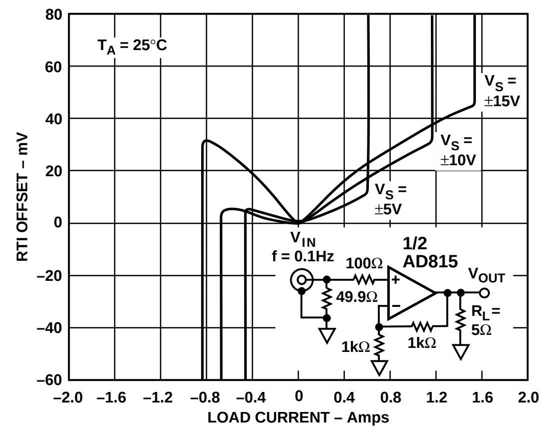


Figure 10. Thermal Nonlinearity vs. Output Current Drive

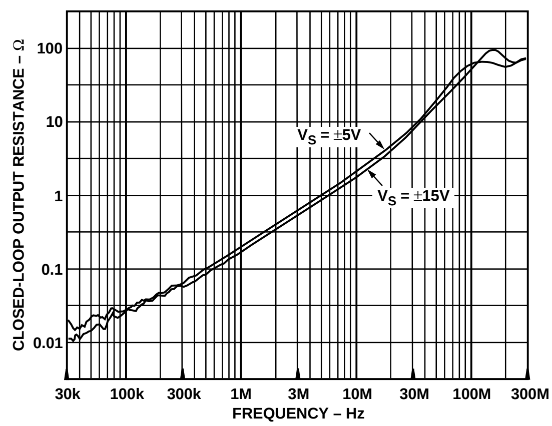


Figure 11. Closed-Loop Output Resistance vs. Frequency

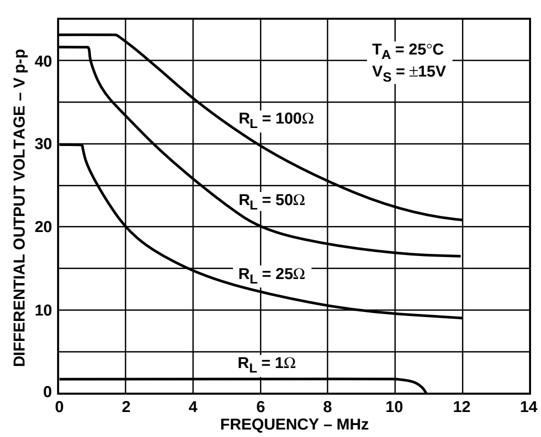


Figure 12. Large Signal Frequency Response

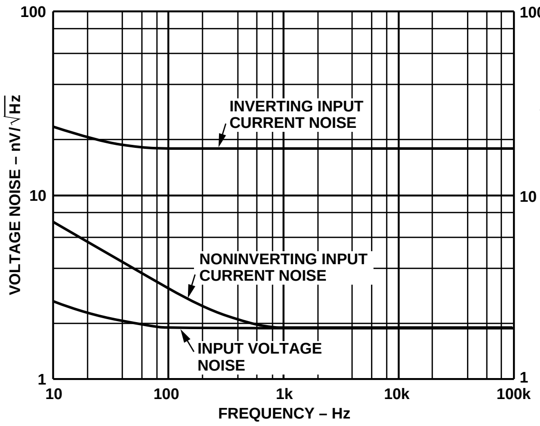


Figure 13. Input Current and Voltage Noise vs. Frequency

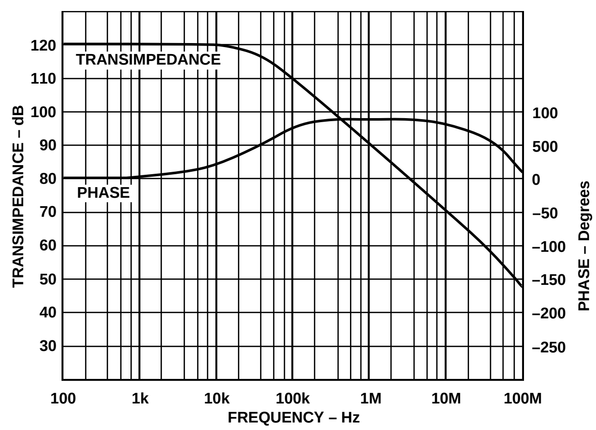


Figure 16. Open-Loop Transimpedance vs. Frequency

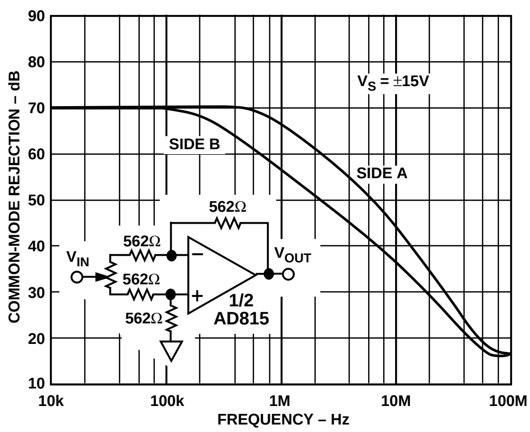


Figure 14. Common-Mode Rejection vs. Frequency

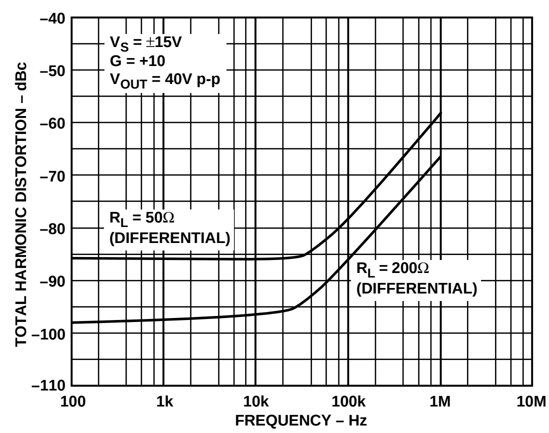


Figure 17. Total Harmonic Distortion vs. Frequency

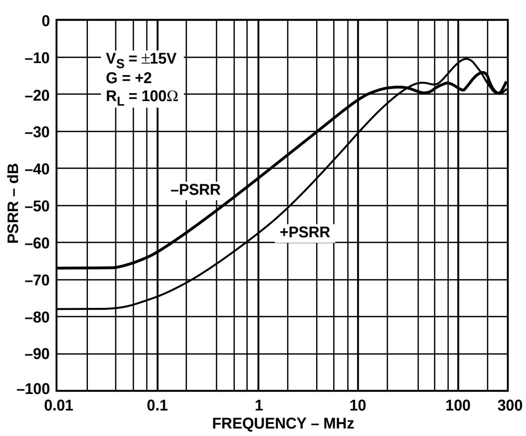


Figure 15. Power Supply Rejection vs. Frequency

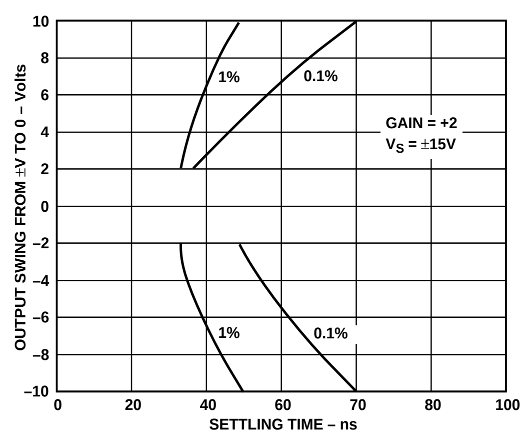


Figure 18. Output Swing and Error vs. Settling Time

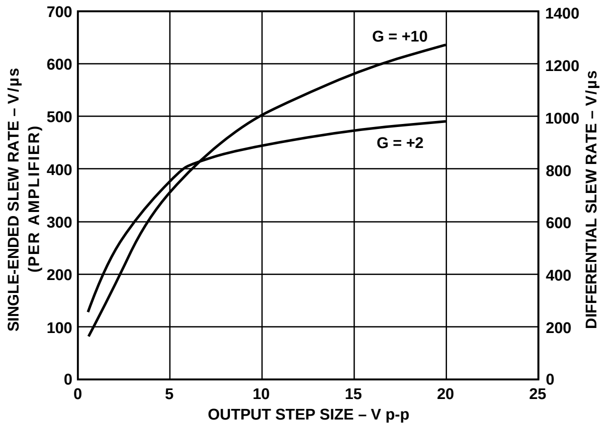


Figure 19. Slew Rate vs. Output Step Size

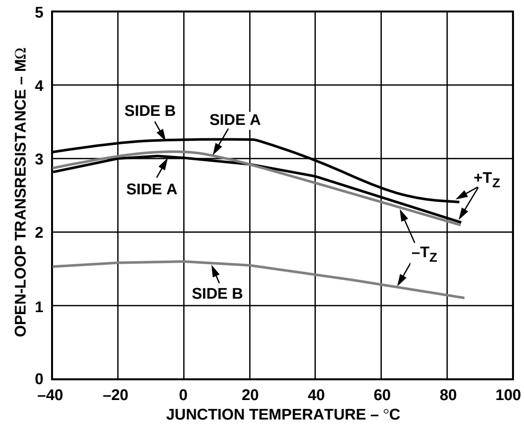


Figure 22. Open-Loop Transresistance vs. Temperature

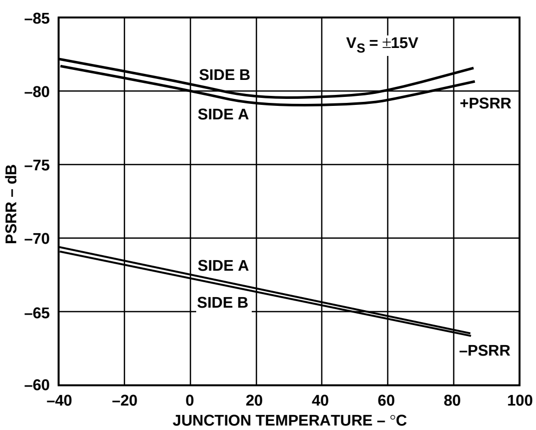


Figure 20. PSRR vs. Temperature

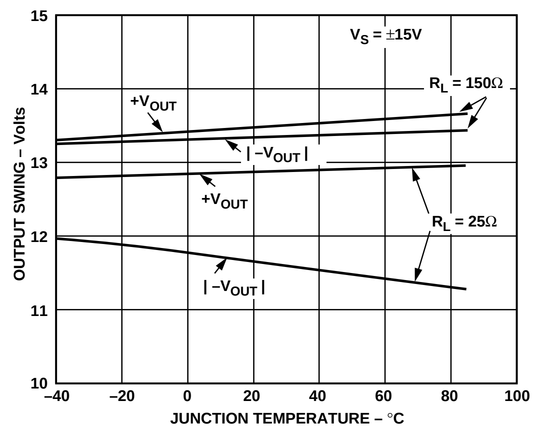


Figure 23. Single-Ended Output Swing vs. Temperature

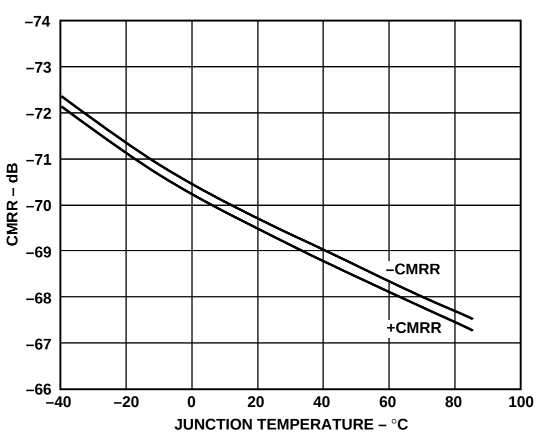


Figure 21. CMRR vs. Temperature

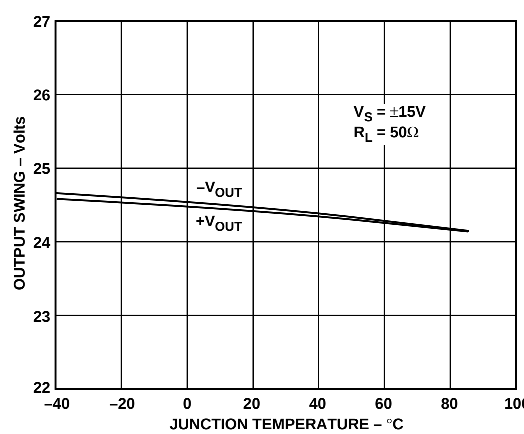


Figure 24. Differential Output Swing vs. Temperature

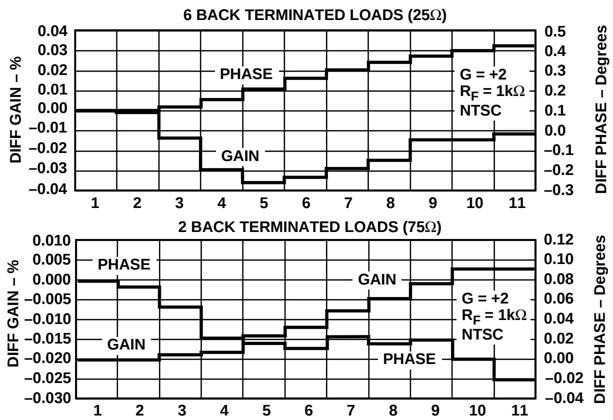


Figure 25. Differential Gain and Differential Phase (per Amplifier)

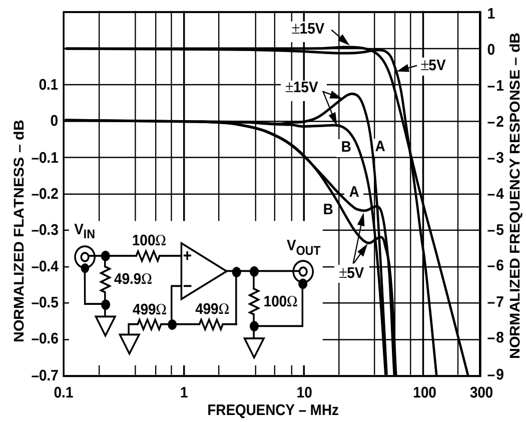


Figure 28. Bandwidth vs. Frequency, G = +2

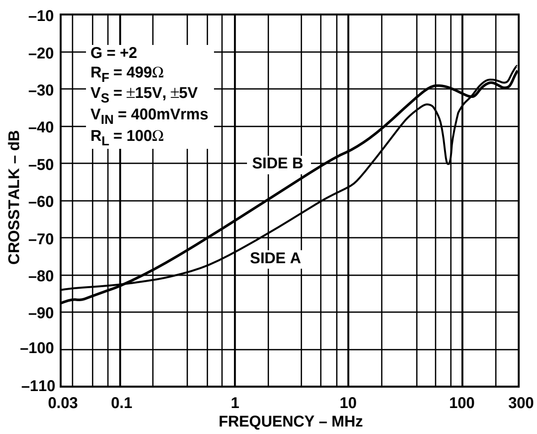


Figure 26. Output-to-Output Crosstalk vs. Frequency

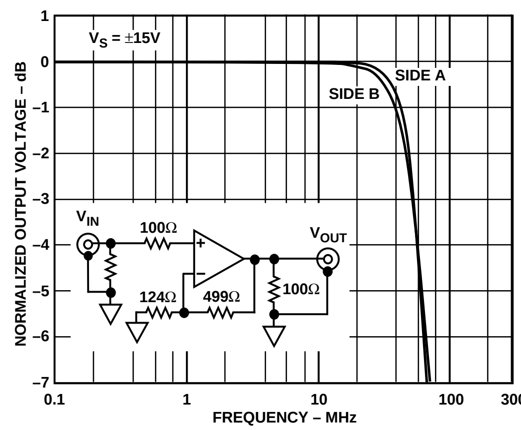


Figure 29. –3 dB Bandwidth vs. Frequency, G = +5

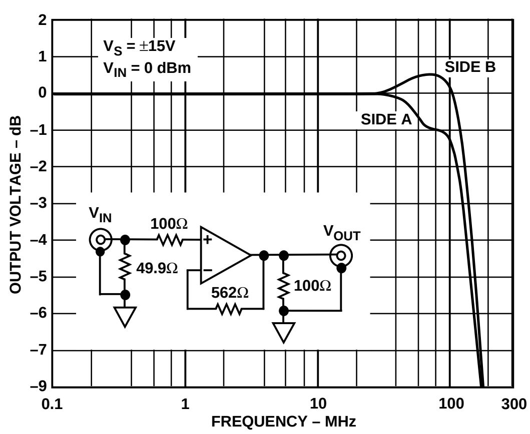


Figure 27. –3 dB Bandwidth vs. Frequency, G = + 1

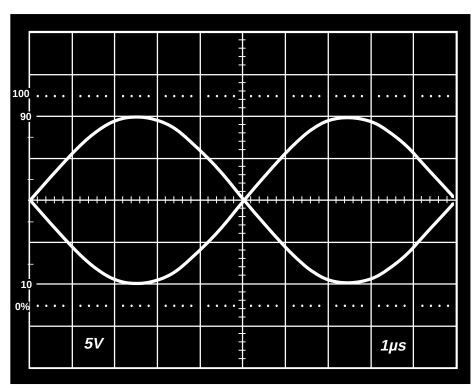


Figure 30. 40 V p-p Differential Sine Wave, R_L = 50 Ω, f = 100 kHz

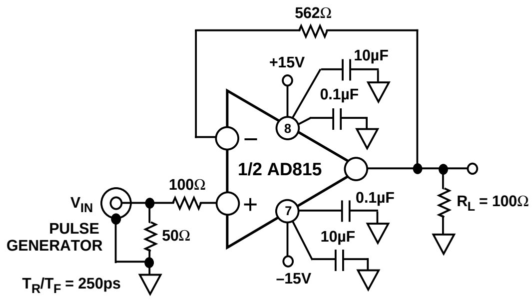


Figure 31. Test Circuit, Gain = +1

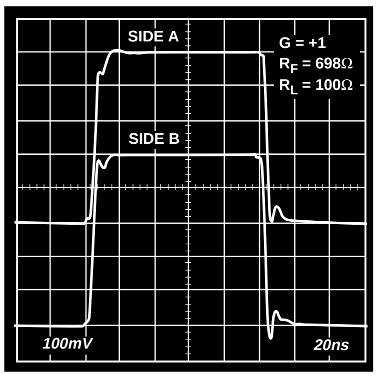


Figure 32. 500 mV Step Response, G = +1

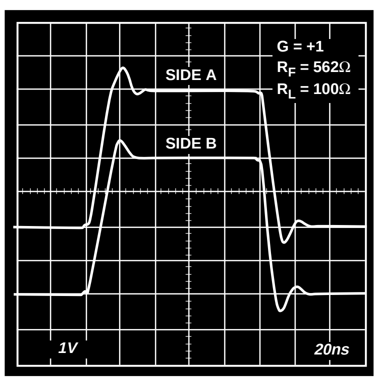


Figure 33. 4 V Step Response, G = + 1

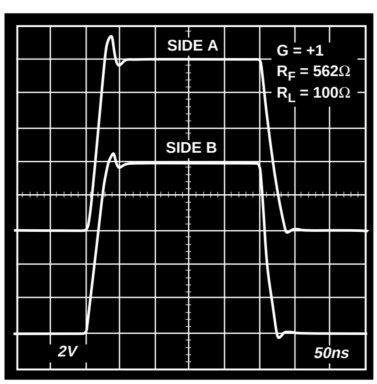


Figure 34. 10 V Step Response, G = + 1

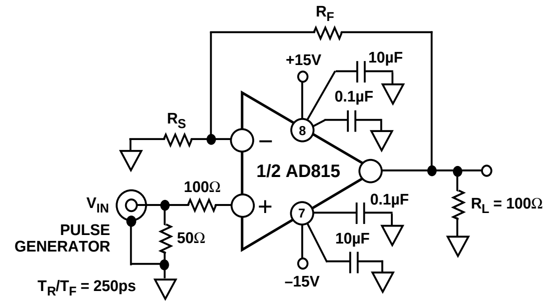


Figure 35. Test Circuit, Gain = 1 + R_F/R_S

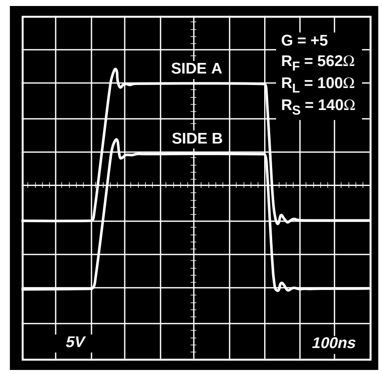


Figure 36. 20 V Step Response, G = +5

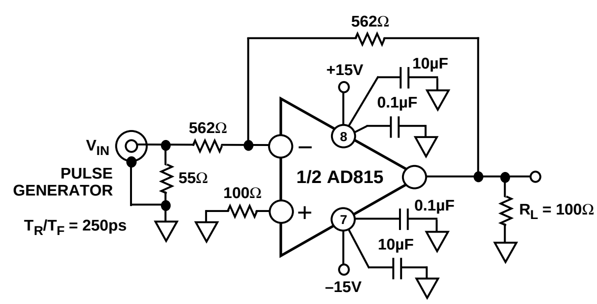


Figure 37. Test Circuit, Gain = –1

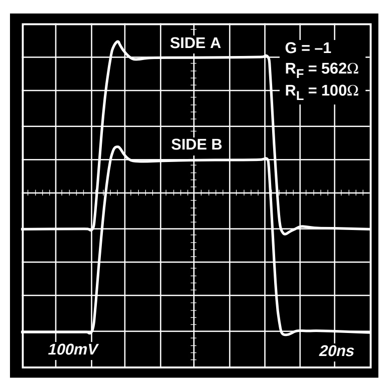


Figure 38. 500 mV Step Response, G = –1

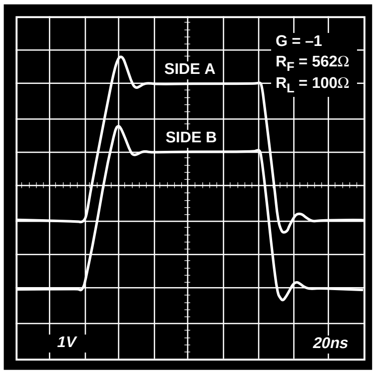


Figure 39. 4 V Step Response, G = –1

THEORY OF OPERATION

The AD815 is a dual current feedback amplifier with high (500 mA) output current capability. Being a current feedback amplifier, the AD815's open-loop behavior is expressed as transimpedance, $\Delta V_O/\Delta I_{-IN}$, or T_Z. The open-loop transimpedance behaves just as the open-loop voltage gain of a voltage feedback amplifier, that is, it has a large dc value and decreases at roughly 6 dB/octave in frequency.

Since R_{IN} is proportional to $1/g_M$, the equivalent voltage gain is just $T_Z \times g_M$, where the g_M in question is the transconductance of the input stage. Using this amplifier as a follower with gain, Figure 40, basic analysis yields the following result:

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + G \times R_{IN} + R_F}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$$R_{IN} = 1/g_M \approx 25\ \Omega$$

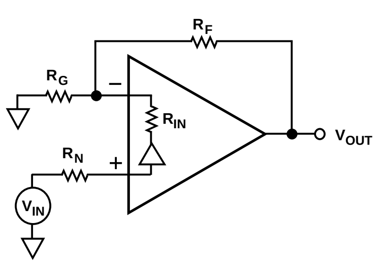


Figure 40.

Recognizing that $G \times R_{IN} << R_F$ for low gains, it can be seen to the first order that bandwidth for this amplifier is independent of gain (G).

Considering that additional poles contribute excess phase at high frequencies, there is a minimum feedback resistance below which peaking or oscillation may result. This fact is used to determine the optimum feedback resistance, R_F. In practice parasitic capacitance at the inverting input terminal will also add phase in the feedback loop, so picking an optimum value for R_F can be difficult.

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

Choice of Feedback and Gain Resistors

The fine scale gain flatness will, to some extent, vary with feedback resistance. It therefore is recommended that once optimum resistor values have been determined, 1% tolerance values should be used if it is desired to maintain flatness over a wide range of production lots. Table I shows optimum values for several useful configurations. These should be used as starting point in any application.

Table I. Resistor Values

		R_F (Ω)	R_G (Ω)
G =	+1	562	∞
	–1	499	499
	+2	499	499
	+5	499	125
	+10	1K	110

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed-loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, a space (5 mm min) should be left around the signal lines to minimize coupling.

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. A parallel combination of 10.0 μF and 0.1 μF is recommended. Under some low frequency applications, a bypass capacitance of greater than 10 μF may be necessary. Due to the large load currents delivered by the AD815, special consideration must be given to careful bypassing. The ground returns on both supply bypass capacitors as well as signal common must be "star" connected as shown in Figure 41.

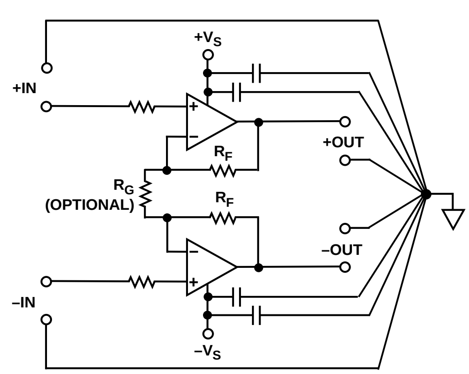


Figure 41. Signal Ground Connected in "Star" Configuration

DC ERRORS AND NOISE

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors refer to the equation below. For noise error the terms are root-sum-squared to give a net output error. In the circuit below (Figure 42), they are input offset (V_{IO}) which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_G$), noninverting input current ($I_{BN} \times R_N$) also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_G and subsequently multiplied by the noise gain always appear at the output as $I_{BI} \times R_F$. The input voltage noise of the AD815 is less than 2 nV/$\sqrt{Hz}$. At low gains though, the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to better offset and drift specifica-tions for the AD815 compared to many other current feedback amplifiers. The typical performance curves in conjunction with the equations below can be used to predict the performance of the AD815 in any application.

$$V_{OUT} = V_{IO} \times \left(1 + \frac{R_F}{R_G}\right) \pm I_{BN} \times R_N \times \left(1 + \frac{R_F}{R_G}\right) \pm I_{BI} \times R_F$$

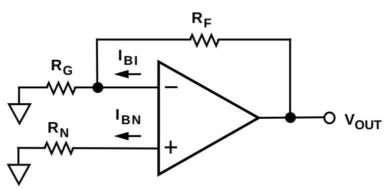


Figure 42. Output Offset Voltage

POWER CONSIDERATIONS

The 500 mA drive capability of the AD815 enables it to drive a 50 Ω load at 40 V p-p when it is configured as a differential driver. This implies a power dissipation, P_{IN}, of nearly 5 watts. To ensure reliability, the junction temperature of the AD815 should be maintained at less than 175°C. For this reason, the AD815 will require some form of heat sinking in most applica-tions. The thermal diagram of Figure 43 gives the basic relationship between junction temperature (T_J) and various components of θ_{JA}.

$$T_J = T_A + P_{IN}\ \theta_{JA} \qquad \text{Equation 1}$$

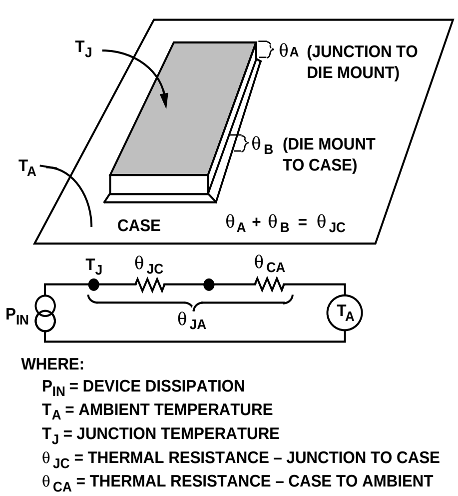


Figure 43. A Breakdown of Various Package Thermal Resistances

Figure 44 gives the relationship between output voltage swing into various loads and the power dissipated by the AD815 (P_{IN}). This data is given for both sine wave and square wave (worst case) conditions. It should be noted that these graphs are for mostly resistive (phase < ±10°) loads. When the power dissipation requirements are known, Equation 1 and the graph on Figure 45 can be used to choose an appropriate heat sinking configuration.

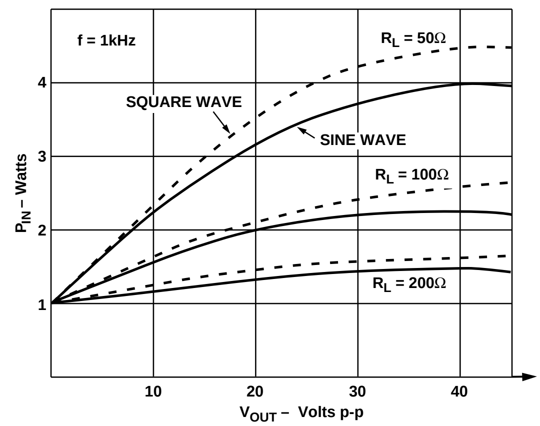


Figure 44. Total Power Dissipation vs. Differential Output Voltage

Normally, the AD815 will be soldered directly to a copper pad. Figure 45 plots θ_{JA} against size of copper pad. This data pertains to copper pads on both sides of G10 epoxy glass board connected together with a grid of feedthroughs on 5 mm centers.

This data shows that loads of 100 ohms or less will usually not require any more than this. This is a feature of the AD815's 15-lead power SIP package.

An important component of θ_{JA} is the thermal resistance of the package to heatsink. The data given is for a direct soldered connection of package to copper pad. The use of heatsink grease either with or without an insulating washer will increase this number. Several options now exist for dry thermal connec-tions. These are available from Bergquist as part # SP600-90. Consult with the manufacturer of these products for details of their application.

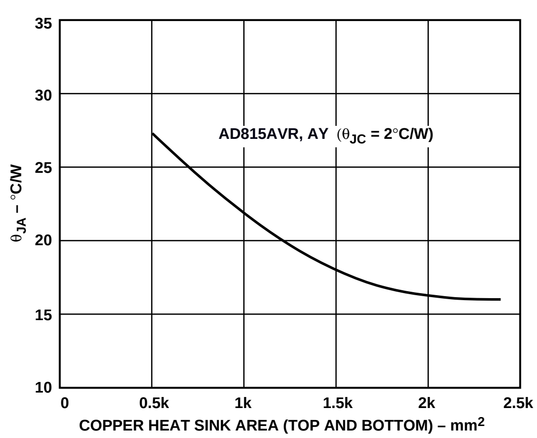


Figure 45. Power Package Thermal Resistance vs. Heat Sink Area

Other Power Considerations

There are additional power considerations applicable to the AD815. First, as with many current feedback amplifiers, there is an increase in supply current when delivering a large peak-to-peak voltage to a resistive load at high frequencies. This behavior is affected by the load present at the amplifier's output. Figure 12 summarizes the full power response capabilities of the AD815. These curves apply to the differential driver applications (e.g., Figure 49 or Figure 53). In Figure 12, maximum continuous peak-to-peak output voltage is plotted vs. frequency for various resistive loads. Exceeding this value on a continuous basis can damage the AD815.

The AD815 is equipped with a thermal shutdown circuit. This circuit ensures that the temperature of the AD815 die remains below a safe level. In normal operation, the circuit shuts down the AD815 at approximately 180°C and allows the circuit to turn back on at approximately 140°C. This built-in hysteresis means that a sustained thermal overload will cycle between power-on and power-off conditions. The thermal cycling typically occurs at a rate of 1 ms to several seconds, depending on the power dissipation and the thermal time constants of the package and heat sinking. Figures 46 and 47 illustrate the thermal shutdown operation after driving OUT1 to the + rail, and OUT2 to the – rail, and then short-circuiting to ground each output of the AD815. The AD815 will not be damaged by momentary operation in this state, but the overload condition should be removed.

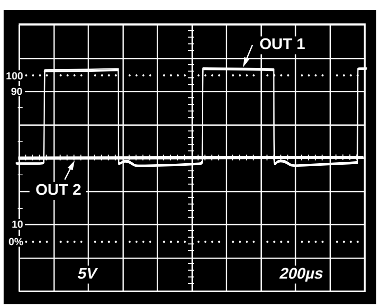


Figure 46. OUT2 Shorted to Ground, Square Wave Is OUT1, R_F = 1 kΩ, R_G = 222 Ω

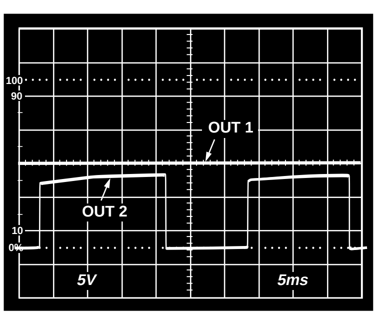


Figure 47. OUT1 Shorted to Ground, Square Wave Is OUT2, R_F = 1 kΩ, R_G = 222 Ω

Parallel Operation

To increase the drive current to a load, both of the amplifiers within the AD815 can be connected in parallel. Each amplifier should be set for the same gain and driven with the same signal. In order to ensure that the two amplifiers share current, a small resistor should be placed in series with each output. See Figure 48. This circuit can deliver 800 mA into loads of up to 12.5 Ω.

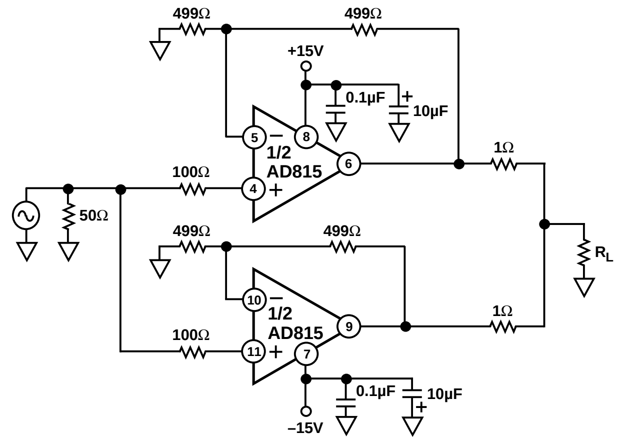


Figure 48. Parallel Operation for High Current Output

Differential Operation

Various circuit configurations can be used for differential operation of the AD815. If a differential drive signal is available, the two halves can be used in a classic instrumentation configuration to provide a circuit with differential input and output. The circuit in Figure 49 is an illustration of this. With the resistors shown, the gain of the circuit is 11. The gain can be changed by changing the value of R_G. This circuit, however, provides no common-mode rejection.

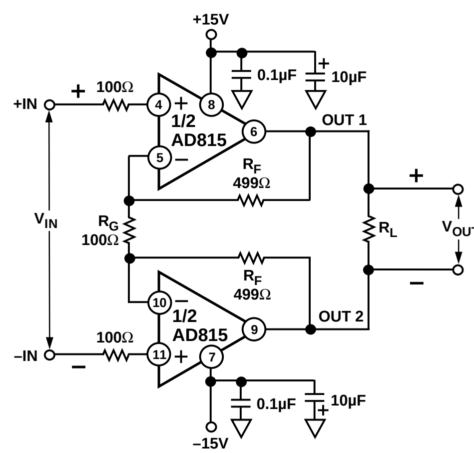


Figure 49. Fully-Differential Operation

Creating Differential Signals

If only a single ended signal is available to drive the AD815 and a differential output signal is desired, several circuits can be used to perform the single-ended to differential conversion.

One circuit to perform this is to use a dual op amp as a predriver that is configured as a noninverter and inverter. The circuit shown in Figure 50 performs this function. It uses an AD826 dual op amp with the gain of one amplifier set at +1 and the gain of the other at –1. The 1 kΩ resistor across the input terminals of the follower makes the noise gain (NG = 1) equal to the inverter's. The two outputs then differentially drive the inputs to the AD815 with no common-mode signal to first order.

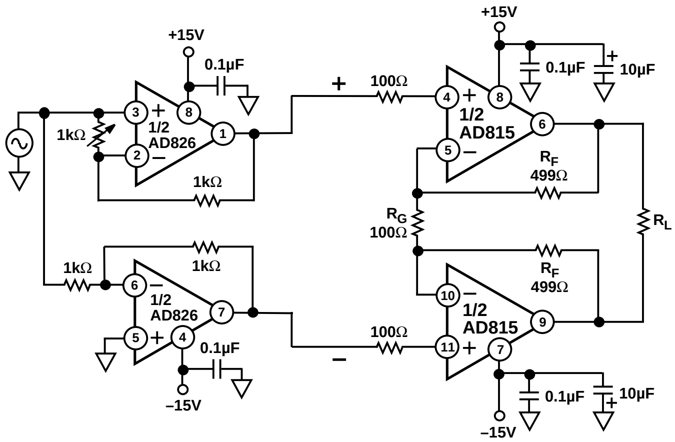


Figure 50. Differential Driver with Single-Ended Differential Converter

Another means for creating a differential signal from a single-ended signal is to use a transformer with a center-tapped secondary. The center tap of the transformer is grounded and the two secondary windings are connected to obtain opposite polarity signals to the two inputs of the AD815 amplifiers. The bias currents for the AD815 inputs are provided by the center tap ground connection through the transformer windings.

One advantage of using a transformer is its ability to provide isolation between circuit sections and to provide good common-mode rejection. The disadvantages are that transformers have no dc response and can sometimes be large, heavy and expensive. This circuit is shown in Figure 51.

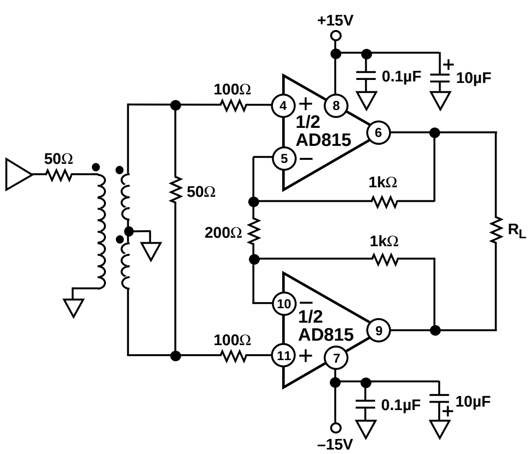


Figure 51. Differential Driver with Transformer Input

Direct Single-Ended to Differential Conversion

Two types of circuits can create a differential output signal from a single-ended input without the use of any other components other than resistors. The first of these is illustrated in Figure 52.

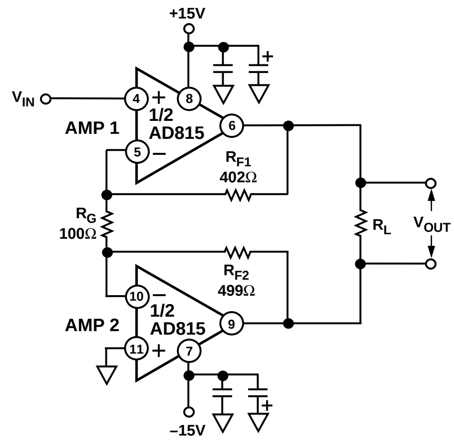


Figure 52. Direct Single-Ended to Differential Conversion

Amp 1 has its + input driven with the input signal, while the + input of Amp 2 is grounded. Thus the – input of Amp 2 is driven to virtual ground potential by its output. Therefore Amp 1 is configured for a noninverting gain of five, $(1 + R_{F1}/R_G)$, because R_G is connected to the virtual ground of Amp 2's – input.

When the + input of Amp 1 is driven with a signal, the same signal appears at the – input of Amp 1. This signal serves as an input to Amp 2 configured for a gain of –5, $(-R_{F2}/R_G)$. Thus the two outputs move in opposite directions with the same gain and create a balanced differential signal.

This circuit can work at various gains with proper resistor selection. But in general, in order to change the gain of the circuit, at least two resistor values will have to be changed. In addition, the noise gain of the two op amps in this configuration will always be different by one, so the bandwidths will not match.

A second circuit that has none of the disadvantages mentioned in the above circuit creates a differential output voltage feedback op amp out of the pair of current feedback op amps in the AD815. This circuit, drawn in Figure 53, can be used as a high power differential line driver, such as required for ADSL (asymmetrical digital subscriber loop) line driving.

Each of the AD815's op amps is configured as a unity gain follower by the feedback resistors (R_A). Each op amp output also drives the other as a unity gain inverter via the two R_Bs, creating a totally symmetrical circuit.

If the + input to Amp 2 is grounded and a small positive signal is applied to the + input of Amp 1, the output of Amp 1 will be driven to saturation in the positive direction and the output of Amp 2 driven to saturation in the negative direction. This is similar to the way a conventional op amp behaves without any feedback.

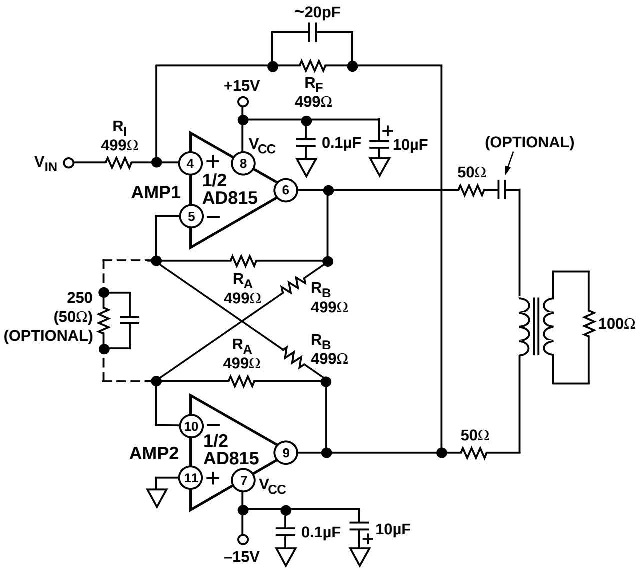


Figure 53. Single-Ended to Differential Driver

If a resistor (R_F) is connected from the output of Amp 2 to the + input of Amp 1, negative feedback is provided which closes the loop. An input resistor (R_I) will make the circuit look like a conventional inverting op amp configuration with differential outputs. The inverting input to this dual output op amp becomes Pin 4, the positive input of Amp 1.

The gain of this circuit from input to either output will be $\pm R_F/R_I$. Or the single-ended to differential gain will be $2 \times R_F/R_I$.

The differential outputs can be applied to the primary of a transformer. If each output can swing ±10 V, the effective swing on the transformer primary is 40 V p-p. The optional capacitor can be added to prevent any dc current in the transformer due to dc offsets at the output of the AD815.

Twelve Channel Video Distribution Amplifier

The high current of the AD815 enables it to drive up to twelve standard 75 Ω reverse terminated video loads. Figure 54 is a schematic of such an application.

The input video signal is terminated in 75 Ω and applied to the noninverting inputs of both amplifiers of the AD815. Each amplifier is configured for a gain of two to compensate for the divide-by-two feature of each cable termination. Six separate 75 Ω resistors for each amplifier output are used for the cable back termination. In this manner, all cables are relatively independent of each other and small disturbances on any cable will not have an effect on the other cables.

When driving six video cables in this fashion, the load seen by each amplifier output is resistive and is equal to 150 Ω/6 or 25 Ω. The differential gain is 0.05% and the differential phase is 0.45°.

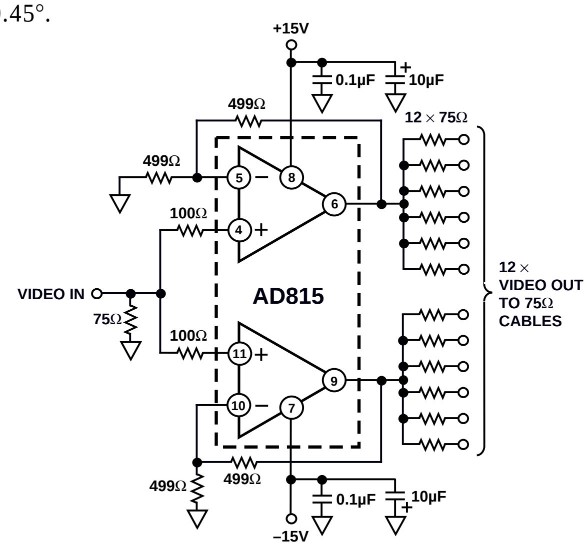


Figure 54. AD815 Video Distribution Amp Driving 12 Video Cables

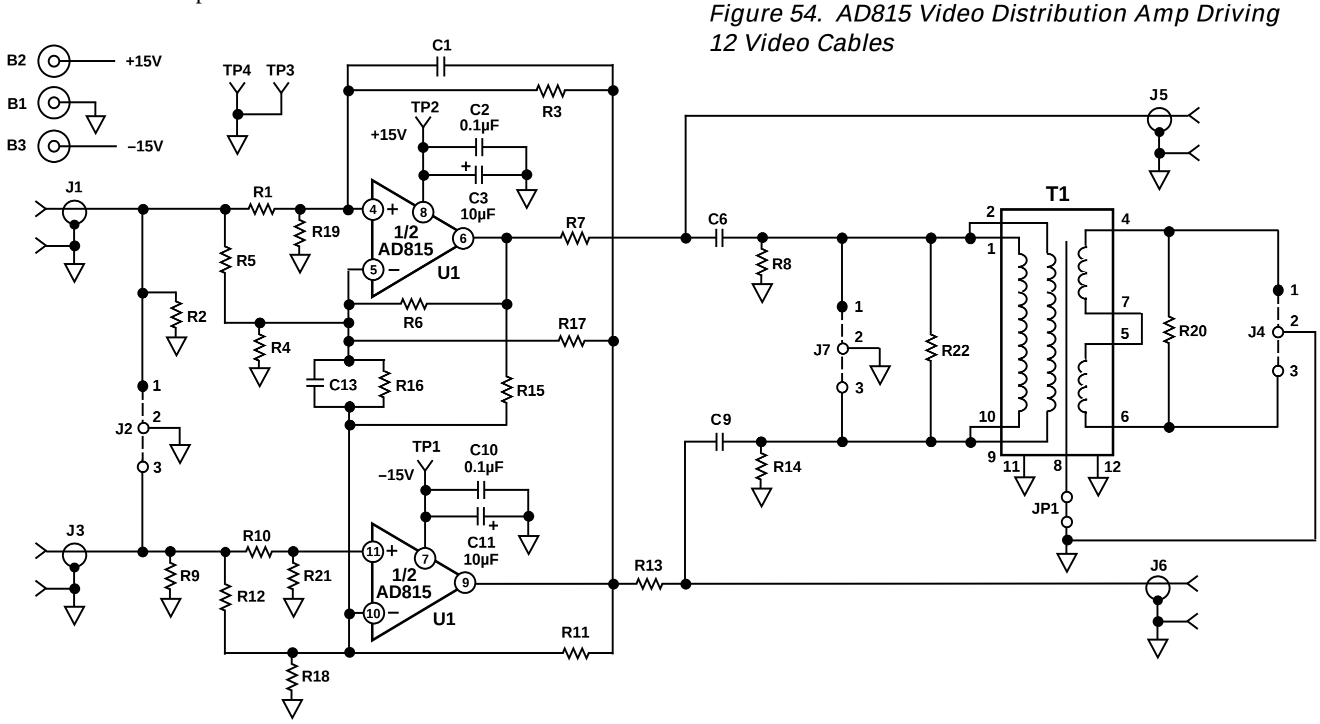


Figure 55. AD815 Evaluation Board Schematic

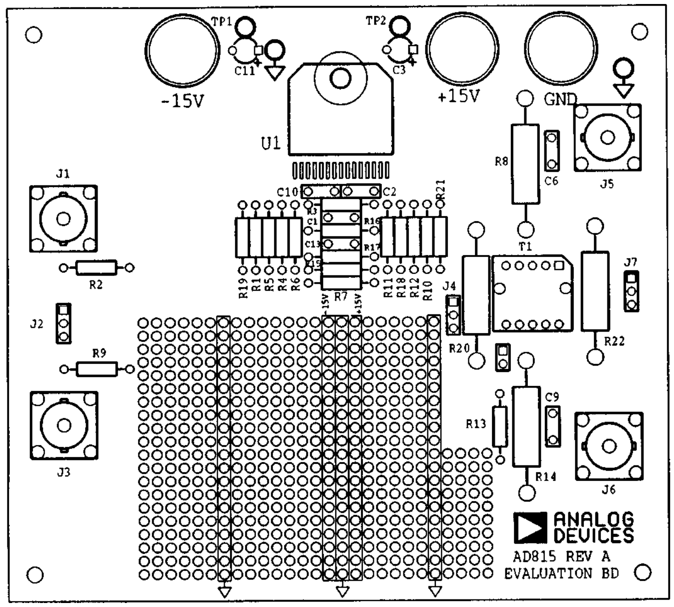


Figure 56. AD815 AVR Evaluation Board Assembly Drawing

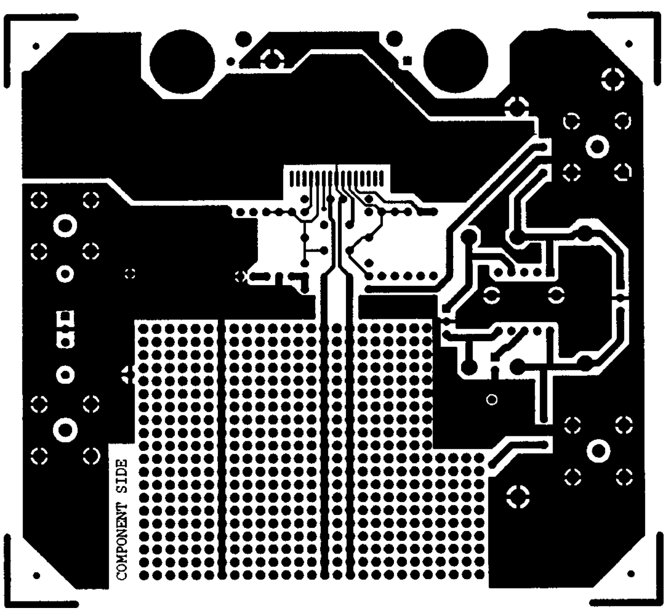


Figure 57. AD815 AVR Evaluation Board Layout (Component Side)

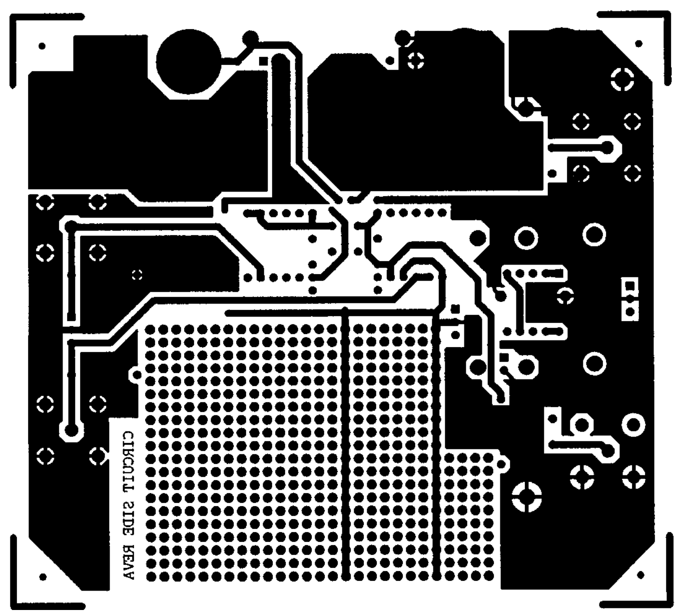
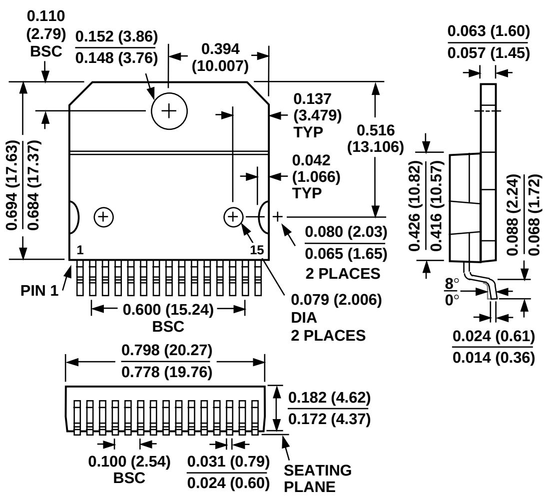


Figure 58. AD815 AVR Evaluation Board Layout (Solder Side)

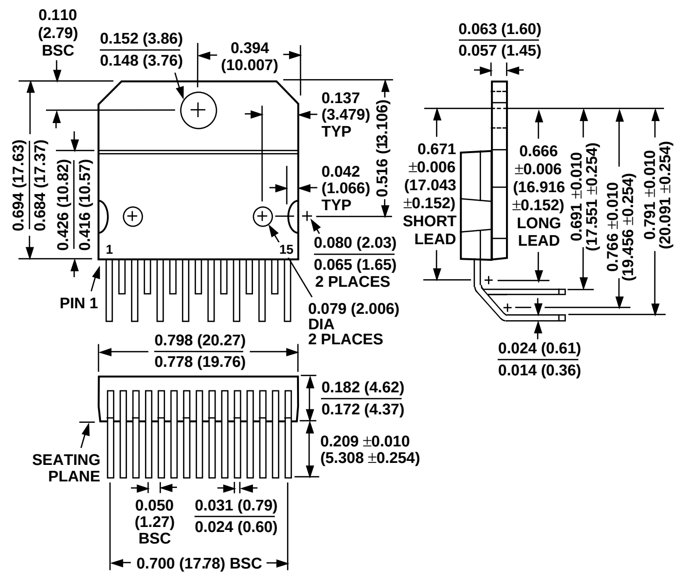
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

15-Pin Surface Mount DDPAK (VR-15)

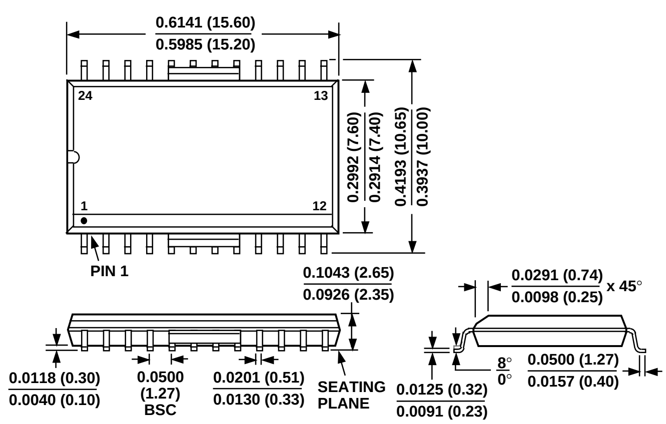


15-Pin Through Hole SIP with Staggered Leads (Y-15)



C2106–15–1/96

24-Pin Thermally Enhanced SOIC (RB-24)



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